|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction ID** | **Inst.** | **Opcode** | **RegDst** | **ALUSrc** | **MemToReg** | **RegWrite** | **Branch**  **Equal** | **Branch**  **Not**  **Equal** | **Jump** | **MemRead** | **MemWrite** |
| **C** | **sub** | **0000** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **I** | **sll** | **0001** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **M** | **sw** | **0010** | **x** | **1** | **x** | **0** | **0** | **0** | **0** | **0** | **1** |
| **B** | **addi** | **0011** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **L** | **lw** | **0100** | **0** | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **0** |
| **E** | **and** | **0101** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **H** | **ori** | **0110** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **D** | **subi** | **0111** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **A** | **add** | **1000** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **G** | **or** | **1001** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **O** | **bneq** | **1010** | **x** | **0** | **x** | **0** | **0** | **1** | **0** | **0** | **0** |
| **J** | **srl** | **1011** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **P** | **j** | **1100** | **x** | **x** | **x** | **0** | **0** | **0** | **1** | **0** | **0** |
| **K** | **nor** | **1101** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **F** | **andi** | **1110** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **N** | **beq** | **1111** | **x** | **0** | **x** | **0** | **1** | **0** | **0** | **0** | **0** |

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction ID** | **Inst.** | **Opcode** | **ALU Control Bits** | | | | | | | | | |
| **ALU Operation Name** | **S2** | **S1** | **S0** | **Cin** | **ShiftLeft** | **ShiftRight** |  |  |  |
| **C** | **sub** | **0000** | **Subtraction** | **0** | **0** | **1** | **1** | **0** | **0** | **0** |  |  |
| **I** | **sll** | **0001** | **Shift Left** | **x** | **x** | **x** | **x** | **1** | **0** | **0** |  |  |
| **M** | **sw** | **0010** | **Addition** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |  |  |
| **B** | **addi** | **0011** | **Addition** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |  |  |
| **L** | **lw** | **0100** | **Addition** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |  |  |
| **E** | **and** | **0101** | **AND** | **1** | **0** | **1** | **x** | **0** | **0** | **0** |  |  |
| **H** | **ori** | **0110** | **OR** | **1** | **1** | **0** | **x** | **0** | **0** | **0** |  |  |
| **D** | **subi** | **0111** | **Subtraction** | **0** | **0** | **1** | **1** | **0** | **0** | **0** |  |  |
| **A** | **add** | **1000** | **Addition** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |  |  |
| **G** | **or** | **1001** | **OR** | **1** | **1** | **0** | **x** | **0** | **0** | **0** |  |  |
| **O** | **bneq** | **1010** | **Subtraction** | **0** | **0** | **1** | **1** | **0** | **0** | **0** |  |  |
| **J** | **srl** | **1011** | **Shift Right** | **x** | **x** | **x** | **x** | **0** | **1** | **0** |  |  |
| **P** | **j** | **1100** | **-** | **x** | **x** | **x** | **x** | **0** | **0** | **0** |  |  |
| **K** | **nor** | **1101** | **NOR** | **1** | **1** | **1** | **x** | **0** | **0** | **0** |  |  |
| **F** | **andi** | **1110** | **AND** | **1** | **0** | **1** | **x** | **0** | **0** | **0** |  |  |
| **N** | **beq** | **1111** | **Subtraction** | **0** | **0** | **1** | **1** | **0** | **0** | **0** |  |  |